

We Claim:

1                   1.     A group write slave comprising:  
2                             an identification stage having a first ID input, a second ID input and an ID  
3                   output, wherein said identification stage includes ID logic circuitry for processing said  
4                   first ID input and said second ID input;

5                             a select stage having a select input and a select output, wherein said select  
6                   stage includes select logic circuitry for processing said select input; and

7                             a slave module, wherein said slave module includes a plurality of slave  
8                   inputs communicated with said select output and said ID output, a plurality of slave  
9                   outputs and slave logic circuitry for processing said plurality of slave inputs so as to  
10                  create said plurality of slave outputs.

1                   2.     A group write slave according to claim 1, wherein said ID logic circuitry  
2                   includes an ID comparator and an ID AND gate, wherein said ID comparator is  
3                   communicated with said first ID input, said second ID input and said ID AND gate, and  
4                   wherein said ID AND gate is communicated with said first ID input and said slave  
5                   module.

1                   3.     A group write slave according to claim 2, wherein said select logic circuitry  
2                   includes a group write comparator, an individual select comparator, an OR gate and a  
3                   select AND gate, wherein said group write comparator and said individual select  
4                   comparator are communicated with said select input and said OR gate and wherein said  
5                   select AND gate is communicated with said OR gate, said select input, said ID  
6                   comparator and said slave module.

1           4.     A group write slave according to claim 2, wherein said ID comparator  
2 includes ID comparator logic circuitry which compares said first ID input with said  
3 second ID input.

1           5.     A group write slave according to claim 3, wherein said group write  
2 comparator includes group write logic circuitry for processing said select input so as to  
3 determine whether said group write slave has been selected as a group.

1           6.     A group write slave according to claim 3, wherein said individual select  
2 comparator includes individual select logic circuitry for processing said select input so as  
3 to determine whether said group write slave has been selected as an individual.

1           7.     A group write slave according to claim 1, wherein said first ID input is  
2 communicated with a master so as to allow communication of a first master signal,  
3 wherein said first master signal includes slave address information and slave ID  
4 information.

1           8.     A group write slave according to claim 1, wherein said second ID input is  
2 communicated with a master so as to allow communication of a second master signal,  
3 wherein said second master signal includes group write identification information.

1           9.     A group write slave according to claim 1, wherein said select input is  
2 communicated with a master so as to allow communication of a third master signal,  
3 wherein said third master signal includes group write command information.

1           10.    A group write slave according to claim 1, wherein at least one of said  
2 plurality of slave outputs is communicated with a type one status bus.

1           11.     A group write slave according to claim 1, wherein at least one of said  
2 plurality of slave outputs is communicated with a type two status bus.

1           12.     A group write slave according to claim 1, wherein at least one of said  
2 plurality of slave outputs includes a slave wait signal and a slave rearbitrate signal and is  
3 communicated with a type three status bus.

1           13.     A group write slave according to claim 1, wherein at least one of said  
2 plurality of slave outputs is responsive to a group wait signal, wherein said group wait  
3 signal is generated through a logical operation conducted external to said group write  
4 slave.

1           14.     A group write slave design according to claim 1, wherein at least one of  
2 said plurality of slave outputs is responsive to a group rearbitrate signal, wherein said  
3 group rearbitrate signal is generated through a logical operation conducted external to  
4 said group write slave.

1                   15.    A sequence alignment logic module comprising:  
2                            a plurality of SAL inputs for receiving a plurality of SAL input signals  
3 from a plurality of group write slaves;  
4                            at least one SAL output for communicating at least one SAL output signal;  
5 and  
6                            a gated logic portion, said gated logic portion having logic circuitry  
7 communicated with said plurality of SAL inputs and said SAL output, wherein said logic  
8 circuitry is constructed so as to create said SAL output signal by sequencing and  
9 combining said plurality of SAL input signals so as to represent the slowest of said  
10 plurality of SAL input signals.

1                   16.    A sequence alignment logic module according to claim 15, wherein said  
2 plurality of SAL inputs includes a first SAL input and a second SAL input.

1                   17.    A sequence alignment logic module according to claim 16, further  
2 comprising a first multiplexor having a first multiplexor select input, a first data input, a  
3 first GRL data input and a first multiplexor output, wherein said first data input is  
4 communicated with said first SAL input and wherein said first GRL data input is  
5 communicated with said SAL output port.

1                   18.    A sequence alignment logic module according to claim 17, further  
2 comprising a second multiplexor having a second multiplexor select input, a second data  
3 input, a second GRL data input and a second multiplexor output, wherein said second  
4 data input is communicated with said second SAL input and wherein said second GRL  
5 data input is forced to a logic zero.

1                   19.     A sequence alignment logic module according to claim 16, further  
2     comprising a first multiplexor having a first multiplexor select input and a first  
3     multiplexor output, wherein when said first multiplexor select input is held to one of  
4     either a logic high or a logic low state, said first multiplexor output is equal to said first  
5     SAL input and wherein when said first multiplexor select input is held to the other of said  
6     logic high or said logic low state, said first multiplexor output is equal to said SAL  
7     output.

1                   20.     A sequence alignment logic module according to claim 16, further  
2     comprising a second multiplexor having a second multiplexor select input and a second  
3     multiplexor output, wherein when said second multiplexor select input is held to one of  
4     either a logic high or a logic low state, said second multiplexor output is equal to said  
5     second SAL input and wherein when said second multiplexor select input is held to the  
6     other of said logic high or said logic low state, said second multiplexor output is equal to  
7     either of said logic high or said logic low.

1                   21.     A method for using a group write slave and a sequence alignment logic  
2 module comprising:

3                   obtaining a computing system that employs a master, at least one  
4 conventional slave, at least one group write slave, three sequence alignment logic  
5 modules, multiplexor logic circuitry and a processor local bus;

6                   selecting said group write slaves so as to cause said group write slave to  
7 create a slave response;

8                   applying said slave response to said sequence alignment logic module so  
9 as to create a mixed response;

10                  applying said slave response and said mixed response to said multiplexor  
11 logic circuitry so as to create a multiplexor response;

12                  performing logical operations on said multiplexor response so as to create  
13 a gated OR response having a wait signal and a rearbitrate signal; and

14                  communicating said gated OR response to said master and to said group  
15 write slaves.

1                   22.     A method according to claim 21, wherein said obtaining a computing  
2 system includes obtaining a computing system where said master is communicated with  
3 said processor local bus which is communicated with said conventional slave and said  
4 group write slaves via a command bus and a shared bus.

1                   23.     A method according to claim 21, wherein said obtaining a computing  
2 system includes obtaining a computing system wherein said group write slaves are  
3 communicated with said sequence alignment logic modules, and wherein said sequence  
4 alignment logic modules are communicated with said processor local bus via a type one  
5 status bus, a type two status bus and a type three status bus.

1           24.     A method according to claim 21, wherein said selecting said group write  
2 slaves include operating said computing system so as to cause said master to  
3 communicate slave address information, slave ID information, group ID information,  
4 command information and write data information to said group write slaves.

1           25.     A method according to claim 24, wherein said selecting said group write  
2 slaves includes comparing said slave address information, said slave ID information, said  
3 group ID information and said command information using said group write slaves so as  
4 to select said group write slave.

1           26.     A method according to claim 24, wherein said selecting said group write  
2 slaves further includes applying said command information and said write data  
3 information to said group write slaves so as to create a slave response.

1           27.     A method according to claim 21, wherein applying said slave response to  
2 said multiplexor logic circuitry includes generating a multiplexor select signal and  
3 communicating said multiplexor select signal to said multiplexor logic circuitry.

1           28.     A method according to claim 23, wherein said performing logical  
2 operations includes applying said type three status bus to gated OR logic circuitry so as to  
3 produce a plurality said wait signal and said rearbitrate signal.

1           29.     A method according to claim 21, wherein said performing logical  
2 operations includes communicating said wait signal and said rearbitrate signal to said  
3 group write slaves.

1                   30.     A method according to claim 21, wherein said communicating said gated  
2     OR response includes communicating said gated OR response and said slave response to  
3     said master through said Processor Local Bus.